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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/648,276

08/27/2003

Shinya Watanabe

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01/05/2005

SUGHRUE MION, PLLC  
2100 PENNSYLVANIA AVENUE, N.W.  
SUITE 800  
WASHINGTON, DC 20037

EXAMINER

DOLAN, JENNIFER M

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/648,276	<b>Applicant(s)</b> WATANABE ET AL.	
	<b>Examiner</b> Jennifer M. Dolan	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 October 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 28-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 28-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/31/04; 11/5/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Objections*

1. Claim 34 is objected to because of the following informalities:

In line 5, "ship" should be replaced by --chip--.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 28, 29, 32, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,926,586 to Dragone et al.

Regarding claim 28, Dragone discloses a chip manufacturing method, comprising: forming a plurality of elements on a wafer (figure 5), and cutting out a plurality of chips, each chip including one element (column 2, lines 50-57; column 4, lines 1-16), wherein each element includes a substantially arcuate shape (curved boundaries in central/dotted-line region of figure 5); each chip includes a concave boundary line and a convex boundary line that substantially follow an outline of one of the elements (column 4, lines 4-13), and the concave boundary line of one chip is shaped the same as the convex boundary line of another chip (column 4, lines 4-13;

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figure 5; if the chips are separated using a nonlinear cut substantially following the contour line of the elements, then it is apparent that the same cut forms the concave boundary of the upper chip and the convex boundary of the lower chip in figure 5).

Regarding claim 29, Dragone discloses that the chips are cut using a laser beam (column 4, lines 18-25).

Regarding claim 32, Dragone discloses that dicing is used to cut the straight-line portions of the contours (column 4, lines 18-25; only the curved portions are cut with the laser; also see column 2, lines 5-26).

Regarding claim 33, Dragone discloses that a plate is mounted on at least a portion of the chip (column 5, lines 10-15).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dragone et al. in view of U.S. Patent No. 5,776,796 to Distefano et al.

Dragone fails to teach that ultrasonic vibration or hydraulic pressure can be used to cut the chips from the wafer.

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Distefano teaches that laser cutting, ultrasonic vibration, and hydraulic pressure cutting are all well-known and interchangeable means for dicing a chip component (see column 5, lines 19-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the method of Dragone uses ultrasonic vibration or hydraulic pressure for cutting the chips from the wafer, as suggested by Distefano. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use ultrasonic vibration or hydraulic pressure cutting, because Dragone shows that even non-ideal dicing means, such as lasers, are appropriate to use with the methods taught by Dragone (see Dragone, column 4, lines 5-35). Since Distefano teaches that all of a laser, ultrasonic vibrator, or hydraulic jet are well-known and recognized equivalent means for dicing a semiconductor wafer, a person skilled in the art could apply any of these to the methods taught by Distefano with a reasonable expectation of success.

6. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dragone in view of U.S. Patent No. 5,745,631 to Reinker.

Dragone discloses forming a plurality of elements on a wafer (figure 5); cutting out a plurality of first and second chips, each chip having an optical multiplexer element (see column 1, lines 5-10), where the first and second chips have substantially similar contours having a (figure 5; the “first chip” can be taken as the ‘highest chip’ and “the second chip” as ‘the second-highest chip’), wherein each element includes a substantially arcuate shape (curved boundaries in central/dotted-line region of figure 5); each chip includes a concave boundary line and a convex

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boundary line that substantially follow an outline of one of the elements (column 4, lines 4-13), and the concave boundary line of one chip is shaped the same as the convex boundary line of another chip (column 4, lines 4-13; figure 5; if the chips are separated using a nonlinear cut substantially following the contour line of the elements, then it is apparent that the same cut forms the concave boundary of the upper chip and the convex boundary of the lower chip in figure 5).

Dragone does not teach bonding the chips together using an adhesive

Reinker discloses an optical multiplexer formed by stacking chips and flowing an adhesive (column 1, lines 25-45; column 2, lines 1-30; figures 9-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Dragone, such that the chips are stacked, as suggested by Reinker. The rationale is as follows: A person having ordinary skill in the art would have been motivated to stack the chips, because doing so allows for the formation of larger scale OEICs, such that a greater number of wavelengths can be accommodated by a multiplexer (see Reinker, column 1, lines 5-30; column 2, lines 25-30; column 5, lines 45-65).

7. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dragone et al. in view of Reinker as applied to claim 34 above, and further in view of U.S. Patent No. 6,379,909 to Forbes et al.

Dragone fails to suggest that the first chip is cut from a first wafer, and the second chip is cut from a second wafer.

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Forbes teaches a stacked chip structure in which the chips can alternately be cut from the same wafer or from different wafers (column 1, lines 20-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Dragone as modified by Reinker, such that the chips are cut from different substrates, as suggested by Forbes. The rationale is as follows: A person having ordinary skill in the art would have been motivated to cut the chips from different substrates, because bonding chips cut from different substrates is well-known in the art, and provides the advantages of allowing each device to be fabricated according to its individual performance needs or fabrication processes, as is appreciated by one skilled in the art (see Forbes, column 1, lines 25-60). Since the invention of Dragone as modified by Reinker includes lasers operating at different wavelengths, and accompanying waveguides appropriate to such wavelengths (see Reinker, column 1, lines 5-30, column 2, lines 25-30, column 5, lines 45-65), it would be expected by a person having ordinary skill in the art that the waveguides and lasers from each layer of the array should be formed on different substrates, such that the individual emission properties can be optimized.

#### ***Response to Arguments***

8. Applicant's arguments filed 10/25/04 have been fully considered but they are not persuasive.

The applicant argues that Dragone does not teach that the concave boundary line of one chip is shaped the same as the convex boundary line of another chip adjoined on the wafer. The

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applicant further argues that the router's boundary lines have different shapes, and the router elements are not adjoined, but rather are arranged at unnecessary intervals on the wafer.

This is not persuasive, because in Dragone, clearly two adjacent chips are separated along a dicing line between and generally following the contour of the router element, as stated in column 4, lines 1-15. For example, the two lowest chips in figure 5 are separated by a single dicing line arranged between the router elements and generally following the contour of both the upper convex curve of the lower element and the lower concave curve of the upper element (see Dragone, columns 3-5). Hence, the concave boundary of one chip must be the same as the concave boundary of an adjoining chip, because the two chips are directly cut apart at that boundary.

Regarding the argument that the router's boundary lines have different shapes, and that the router elements are not adjoined, these arguments are not persuasive because such elements are not specifically claimed. The claim language only states that the boundary lines of the chip substantially follow the outline of the element. Dragone, however, specifically states that the chips are cut along lines that follow the contours of the router (see column 4, lines 1-13). The claim language further only states that the chips are adjoined, and not the router elements, themselves. Insofar as the claims could be amended to reflect that the routers must be adjoining, the arguments are still not persuasive, because it is apparent from figure 5 and the description (column 3, line 60 – column 4, line 20) that the routers are packed together as tightly as is geometrically feasible, and thus would be considered to be “adjoining.”

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan  
Examiner  
Art Unit 2813

jmd

  
**CRAIG A. THOMPSON**  
**PRIMARY EXAMINER**